PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-260993

(43)Date of publication of application : 22.09.2000

(51)Int.Cl. H01L 29/786

G02F 1/136

H01L 21/336

(21)Application number : 11-062016 (71)Applicant : SEIKO EPSON CORP

(22)Date of filing : 09.03.1999 (72)Inventor : KIMURA MUTSUMI

(54) THIN-FILM TRANSISTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To suppress decrease of on-current by specifying the peak angle of a protrusion on a rough surface present at the interface between a semiconductor film and a gate insulating film to be at least a right angle, or specifying width and height of the protrusion on the rough surface.

SOLUTION: The thin-film transistor comprises a semiconductor film 2 and a gate electrode 4 with a gate insulating film 3 between them. Here, an apex angle A of the protrusion of a rough surface 8 present at the interface between the semiconductor film 2 and the gate insulating film 3 satisfies A>90°. Otherwise, a width W and height H of the protrusion of the rough surface 8 satisfy an equation: (W/2)H>tan(90°/2). Since the shape of the rough surface 8 does not prevent

conduction of carrier, drop of on-current is suppressed.

LEGAL STATUS

[Date of request for examination]	02.07.2003
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	withdrawal
[Date of final disposal for application]	20.12.2004
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The thin film transistor characterized by the vertical angle A of the height of the surface roughness which exists in the interface of said semi-conductor film and said gate dielectric film in a thin film transistor which was equipped with the semi-conductor film and a gate electrode, and was equipped with gate dielectric film between said semi-conductor film and said gate electrodes filling A > 90 degrees.

[Claim 2] The thin film transistor to which the width of face W of the height of the surface roughness which exists in the interface of said semi-conductor film and said gate dielectric film in a thin film transistor and height H which were equipped with the semi-conductor film and a gate electrode, and were equipped with gate dielectric film between said semi-conductor film and said gate electrodes are characterized by filling (W/2) / H > tan (90 degrees / 2).

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a thin film transistor and the thin film transistor which was equipped with the semi-conductor film and a gate electrode, and was especially equipped with gate dielectric film between the semi-conductor film and a gate electrode.

[0002]

[Background of the Invention] In recent years, the thin film transistor is widely used as a means to realize the light and thin indicating equipment represented by a liquid crystal display and the electroluminescence display, or a scanner, a detector and other equipments.

[0003] The structure of a thin film transistor is shown in drawing 1 . The semi-conductor film 2 is formed on a substrate 1, gate dielectric film 3 is formed on it, and the gate electrode 4 is formed on it. After an interlayer insulation film 5 is formed, the source electrode 6 and the drain electrode 7 are formed, and it completes. Refer to S.Inoue, et al, Asia Display95, and p339 for the detailed device structure and detailed process conditions.

[0004] In a thin film transistor, since the semi-conductor film 2 is made to deposit on a substrate and forms by some approaches, such as LPCVD-PECVD and a spatter, it is not avoided by that surface roughness 8 exists in the front face. Surface roughness 8 occurs, so that you may surely say that the semi-conductor film 2 is especially crystallized by laser radiation. Generally, even after forming gate dielectric film 3, it exists as surface roughness 8 of the interface of the semi-conductor film 2 and gate dielectric film 3.

[0005]

[Problem(s) to be Solved by the Invention] The surface roughness 8 which exists in the interface of the semi-conductor film 2 and gate dielectric film 3 checks carrier conduction of a thin film transistor, and we are anxious about it in whether the ON state current is reduced. Then, the purpose of this invention is controlling the carrier conduction inhibition and the ON state current fall by surface

roughness 8.

[0006]

[Means for Solving the Problem] (1) This invention according to claim 1 is a thin film transistor characterized by the vertical angle A of the height of the surface roughness which exists in the interface of the semi-conductor film and gate dielectric film in a thin film transistor which was equipped with the semi-conductor film and a gate electrode, and was equipped with gate dielectric film between the semi-conductor film and a gate electrode filling A > 90 degrees.

[0007] According to this configuration, since surface roughness does not bar conduction of a carrier, the fall of the ON state current does not take place.

[0008] (2) It is the thin film transistor characterized by the width of face W of the height of the surface roughness which exists in the interface of the semi-conductor film and gate dielectric film in a thin film transistor and height H which this invention according to claim 2 was equipped with the semi-conductor film and a gate electrode, and were equipped with gate dielectric film between the semi-conductor film and a gate electrode filling (W/2) / H > tan (90 degrees / 2).

[0009] According to this configuration, since surface roughness does not bar conduction of a carrier, the fall of the ON state current does not take place.

[0010]

[Embodiment of the Invention] Hereafter, the gestalt of desirable operation of this invention is explained.

[0011] Drawing 2 is drawing showing the surface roughness which exists in the interface of the semi-conductor film and gate dielectric film. The height of the height of W and surface roughness is set [the vertical angle of the height of surface roughness] to H for the width of face of the height of A and surface roughness.

[0012] It asked for change of the ON state current by device simulation, changing W and H. The structure of a thin film transistor is as drawing 1 and drawing 2 . They are an n channel, a self aryne, channel length 10um, and spacing 3um of surface roughness 8. Vd=8 V-Vg=12V were impressed. Here, the polycrystal thin

film transistor crystalized by laser radiation is assumed. In addition, although top gate structure explains, the same effectiveness is expectable with other structures here.

[0013] Drawing 3 is the dependency of the ON state current over the vertical angle A of the height of surface roughness. it turns out that width-of-face W and height H of the height of surface roughness boil the ON state current, respectively, and it does not depend for it independently, but is mainly dependent on the vertical angle A of the height of surface roughness. The ON state current will deteriorate rapidly, if the vertical angle A of a height becomes smaller than 90 degrees. Then, the fall of the ON state current can be controlled by the thing which are shown in claim 1 and to consider as like and A > 90 degrees. This originates in surface roughness 8 serving as a configuration which does not bar conduction of a carrier.

[0014] Generally, the configuration of surface roughness 8 is not what [KITCHIRI / what / as shown in drawing 2], and defining the vertical angle A of a height has a difficult thing. In this case, although it is mathematically equivalent, as shown in claim 2, the fall of the ON state current can be controlled by filling (W/2) / H > tan (90 degrees / 2).

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Drawing showing the structure of a thin film transistor.

[Drawing 2] Drawing showing the surface roughness which exists in the interface of the semi-conductor film and gate dielectric film.

[Drawing 3] Drawing showing the dependency of the ON state current over the vertical angle A of the height of surface roughness.

[Description of Notations]

1 Substrate

2 Semi-conductor Film

3 Gate Dielectric Film

4 Gate Electrode

5 Interlayer Insulation Film

6 Source Electrode

7 Drain Electrode

8 Surface Roughness

A The vertical angle of the height of surface roughness

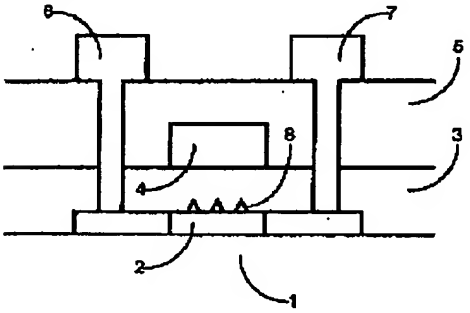
W Width of face of the height of surface roughness

H Height of the height of surface roughness

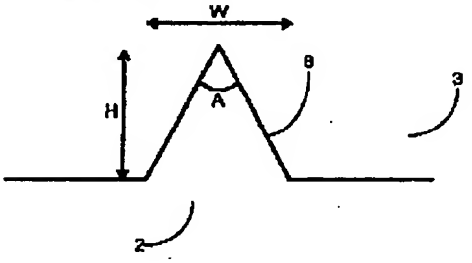
[Translation done.]

DRAWINGS

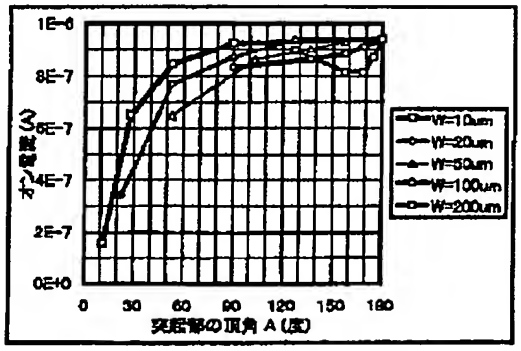
[Drawing 1]



[Drawing 2]



[Drawing 3]



Searching PAJ

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-260993
(43)Date of publication of application : 22.09.2000

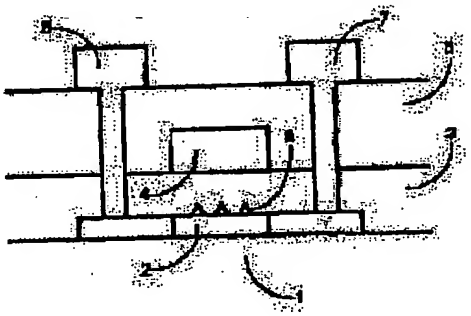
(51)Int.Cl. H01L 29/786
G02F 1/136
H01L 21/336

(21)Application number : 11-062016
(22)Date of filing : 09.03.1999

(71)Applicant : SEIKO EPSON CORP
(72)Inventor : KIMURA MUTSUMI

(54) THIN-FILM TRANSISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress decrease of on-current by specifying the peak angle of a protrusion on a rough surface present at the interface between a semiconductor film and a gate insulating film to be at least a right angle, or specifying width and height of the protrusion on the rough surface.
SOLUTION: The thin-film transistor comprises a semiconductor film 2 and a gate electrode 4 with a gate insulating film 3 between them. Here, an apex angle A of the protrusion of a rough surface 8 present at the interface between the semiconductor film 2 and the gate insulating film 3 satisfies A>90° . Otherwise, a width W and height H of the protrusion of the rough surface 8 satisfy an equation: (W/2)H>tan(90° /2). Since the shape of the rough surface 8 does not prevent conduction of carrier, drop of on-current is suppressed.



LEGAL STATUS

[Date of request for examination]	02.07.2003
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	withdrawal
[Date of final disposal for application]	20.12.2004
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2000－260993
（Ｐ2000－260993Ａ）
(43)公開日　平成12年９月22日(2000.9.22)

(51)Int.Cl.⁷	識別記号	ＦＩ		テーマコード（参考）
Ｈ０１Ｌ　29/786		Ｈ０１Ｌ　29/78	６１８Ｃ	２Ｈ０９２
Ｇ０２Ｆ　1/136	５００	Ｇ０２Ｆ　1/136	５００	５Ｆ１１０
Ｈ０１Ｌ　21/336		Ｈ０１Ｌ　29/78	６１７Ｓ	

審査請求　未請求　請求項の数２　ＯＬ　（全３頁）

(21)出願番号　特願平11－62016

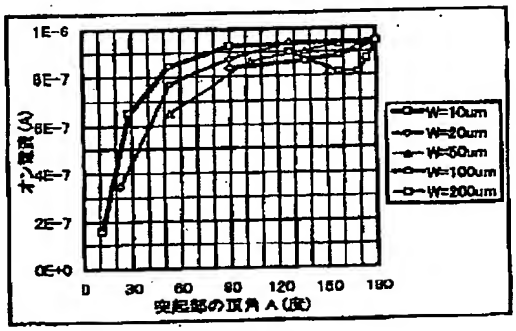
(22)出願日　平成11年３月９日(1999.3.9)

(71)出願人　000002369
セイコーエプソン株式会社
東京都新宿区西新宿２丁目４番１号
(72)発明者　木村　睦
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内
(74)代理人　100093388
弁理士　鈴木　喜三郎　（外２名）

Ｆターム(参考)　2H092 JA25 JA29 JA38 JA42 JA44
JA46 JB13 JB23 JB32 JB33
JB38 KA04 KA07 NA22 NA25
5F110 CC02 GG02 GG13 GG22 GG23
GG28 GG30 PP03 QQ11

(54)【発明の名称】　薄膜トランジスタ

(57)【要約】
【課題】　薄膜トランジスタにおいて、半導体膜とゲート絶縁膜との界面に存在する表面粗さによる、キャリア伝導阻害・オン電流低下を、抑制することを目的とする。
【解決手段】　表面粗さの突起部の頂角Aが、Ａ＞90度、を満たすようにする。表面粗さの突起部の幅Wおよび高さHが、(W/2)/Ｈ＞tan(90度/2)、を満たすようにする。



1

【特許請求の範囲】

【請求項１】 半導体膜とゲート電極とを備え、前記半導体膜と前記ゲート電極との間にゲート絶縁膜を備えた、薄膜トランジスタにおいて、

前記半導体膜と前記ゲート絶縁膜との界面に存在する表面粗さの突起部の頂角Aが、

A > 90度

を満たすことを特徴とする、薄膜トランジスタ。

【請求項２】 半導体膜とゲート電極とを備え、前記半導体膜と前記ゲート電極との間にゲート絶縁膜を備えた、薄膜トランジスタにおいて、

前記半導体膜と前記ゲート絶縁膜との界面に存在する表面粗さの突起部の幅Wおよび高さHが、

(W/2)/H > tan(90度/2)

を満たすことを特徴とする、薄膜トランジスタ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、薄膜トランジスタ、特に、半導体膜とゲート電極とを備え、半導体膜とゲート電極との間にゲート絶縁膜を備えた、薄膜トランジスタに関する。

【０００２】

【背景技術】近年、液晶ディスプレイやエレクトロルミネッセンスディスプレイに代表される軽量･薄型の表示装置、あるいは、スキャナやデテクターやその他の装置を実現する手段として、薄膜トランジスタは、広く用いられている。

【０００３】図１に、薄膜トランジスタの構造を示す。基板1上に半導体膜2が形成され、その上にゲート絶縁膜3が形成され、その上にゲート電極4が形成される。層間絶縁膜5が形成された後、ソース電極6およびドレイン電極7が形成されて、完成する。その詳しいデバイス構造やプロセス条件は、S. Inoue, et al, Asia Display95, p339を参照のこと。

【０００４】薄膜トランジスタにおいては、半導体膜2は、LPCVD･PECVD･スパッタ等、何らかの方法で基板上に堆積させて形成するため、その表面に表面粗さ8が存在するのは避けられない。特に、レーザー照射により半導体膜2の結晶化を行うと、必ずと言ってよいほど、表面粗さ8が発生する。一般に、ゲート絶縁膜3を成膜した後も、半導体膜2とゲート絶縁膜3との界面の表面粗さ8として存在する。

【０００５】

【発明が解決しようとする課題】半導体膜2とゲート絶縁膜3との界面に存在する表面粗さ8は、薄膜トランジスタのキャリア伝導を阻害し、オン電流を低下させるのではないかと、懸念される。そこで、本発明の目的は、表面粗さ8によるキャリア伝導阻害･オン電流低下を、抑制することである。

【０００６】

2

【課題を解決するための手段】（１）請求項１記載の本発明は、半導体膜とゲート電極とを備え、半導体膜とゲート電極との間にゲート絶縁膜を備えた、薄膜トランジスタにおいて、半導体膜とゲート絶縁膜との界面に存在する表面粗さの突起部の頂角Aが、A > 90度、を満たすことを特徴とする、薄膜トランジスタである。

【０００７】本構成によれば、表面粗さが、キャリアの伝導を妨げないので、オン電流の低下が起こらない。

【０００８】（２）請求項２記載の本発明は、半導体膜とゲート電極とを備え、半導体膜とゲート電極との間にゲート絶縁膜を備えた、薄膜トランジスタにおいて、半導体膜とゲート絶縁膜との界面に存在する表面粗さの突起部の幅Wおよび高さHが、(W/2)/H > tan(90度/2)、を満たすことを特徴とする、薄膜トランジスタである。

【０００９】本構成によれば、表面粗さが、キャリアの伝導を妨げないので、オン電流の低下が起こらない。

【００１０】

【発明の実施の形態】以下、本発明の好ましい実施の形態を、説明する。

【００１１】図２は、半導体膜とゲート絶縁膜との界面に存在する表面粗さを示す図である。表面粗さの突起部の頂角をA、表面粗さの突起部の幅をW、表面粗さの突起部の高さをH、とする。

【００１２】デバイスシミュレーションにより、WおよびHを変化させながら、オン電流の変化を求めた。薄膜トランジスタの構造は、図１･図２のとおりである。 nチャネル、セルフアライン、チャネル長10um、表面粗さ8の間隔3umである。Vd＝8V･Vg=12Vを印加した。ここでは、レーザー照射により結晶化した多結晶薄膜トランジスタを想定している。なお、ここでは、トップゲート構造で説明しているが、他の構造でも同じ効果が期待できる。

【００１３】図３は、表面粗さの突起部の頂角Aに対する、オン電流の依存性である。オン電流は、表面粗さの突起部の幅W･高さHのそれぞれに独立に依存するのではなく、主に、表面粗さの突起部の頂角Aに依存していることがわかる。オン電流は、突起部の頂角Aが90度より小さくなると、急激に劣化する。そこで、請求項１に示すように、 A > 90度、とすることで、オン電流の低下を抑制することができる。これは、表面粗さ8が、キャリアの伝導を妨げない形状となっていることに起因する。

【００１４】一般に、表面粗さ8の形状は、図２に示すようにキッチリしたものではなく、突起部の頂角Aを定義するのは難しいことがある。この場合は、数学的には等価であるが、請求項２に示すように、(W/2)/H > tan(90度/2)、を満たすことで、オン電流の低下を抑制することができる。

【図面の簡単な説明】

【図１】薄膜トランジスタの構造を示す図。

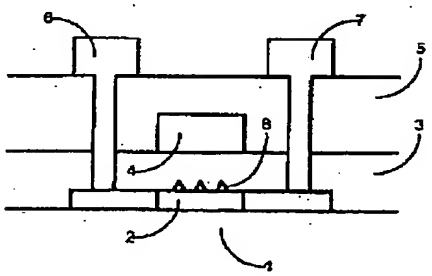
【図２】半導体膜とゲート絶縁膜との界面に存在する表面粗さを示す図。

【図３】表面粗さの突起部の頂角Aに対するオン電流の依存性を示す図。

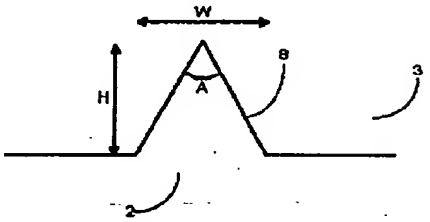
【符号の説明】

1　基板
2　半導体膜
3．ゲート絶縁膜
4　ゲート電極
5　層間絶縁膜
6　ソース電極
7　ドレイン電極
8　表面粗さ
A　表面粗さの突起部の頂角
W　表面粗さの突起部の幅
H　表面粗さの突起部の高さ

【図１】



【図２】



【図３】